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PATENT
5500-05001/TT1915D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/217,213

Filed: December 21, 1998

Inventors:

Mark I. Gardner

H. Jim Fulford

Derick J. Wristers


Title: Semiconductor Fabrication
Employing Implantation of
Excess Atoms at the Edges
of a Trench Isolation
Structure

§ Examiner: Mai, Anh D.
§ Group/Art Unit: 2814
§ Atty. Dkt. No: 5500-05001
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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Robert C. Kowert

Printed Name


Signature Date

December 21, 2004

**RESPONSE TO OFFICE ACTION OF
SEPTEMBER 21, 2004**

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Office Action of September 21, 2004, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.